WEST

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L3: Entry 1 of 1   File: DWPI   Jan 24, 1995

DERWENT-ACC-NO: 1995-095510
DERWENT-WEEK: 199513
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TITLE: Semiconductor IC apparatus manufacturing method for MOSFET - involves
shortening the channel length, while channel width of MOSFET is enlarged and metal
layer is formed along with gate electrode

PATENT-ASSIGNEE:

ASSIGNEE	CODE
HITACHI LTD	HITA
NIPPON TEXAS INSTR KK	TEXI

PRIORITY-DATA: 1993JP-0190891 (July 2, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 07022516 A	January 24, 1995		006	H01L021/8234

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
JP 07022516A	July 2, 1993	1993JP-0190891	

INT-CL (IPC): H01 L 21/82; H01 L 21/8234; H01 L 21/8242; H01 L 27/088; H01 L 27/108

ABSTRACTED-PUB-NO: JP 07022516A
BASIC-ABSTRACT:

The semiconductor IC apparatus manufacturing method involves shortening of channel
length while the channel width of MOSFET is extended. Along with the gate electrode
of the MOSFET, a metal wiring layer is formed through an insulating film in the
upper part. The input signal is supplied from both ends of the gate electrodes.

ADVANTAGE - Realises improvement in speed without increasing area.

CHOSEN-DRAWING: Dwg.1/5

TITLE-TERMS: SEMICONDUCTOR IC APPARATUS MANUFACTURE METHOD MOSFET SHORTENING CHANNEL
LENGTH CHANNEL WIDTH MOSFET ENLARGE METAL LAYER FORMING GATE ELECTRODE

DERWENT-CLASS: U11 U13

EPI-CODES: U11-D03C; U13-C02A; U13-D02;

SECONDARY-ACC-NO:
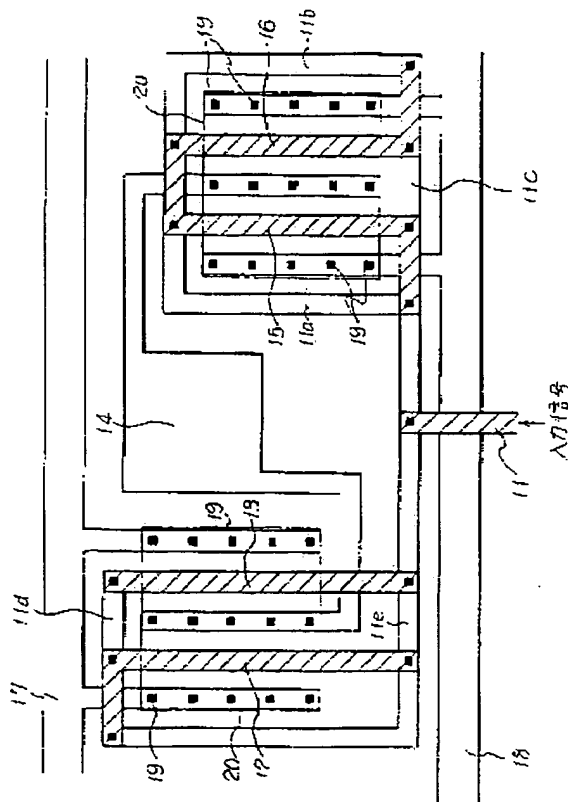Non-CPI Secondary Accession Numbers: N1995-075299

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** Result [Utility-model] ** Format(P803) 06.Nov.2003        1/        1

    Application no/date:                    1984-128916[1984/08/24]
    Date of request for examination:        [              ]
    Public disclosure no/date:              1986- 44854[1986/03/25]
    Examined publication no/date (old law):         [         ]
    Registration no/date:                           [         ]
    Examined publication date (present law):        [         ]
    PCT application no
    PCT publication no/date                  [          ]
    Applicant: NEC CORP
    Inventor:  YASUDA SADAHIRO
    IPC:    H01L 27/08   ,102   H01L 29/78
    FI:     H01L 27/08   ,321L H01L 29/78
    F-term:  5F048AA00,AB04,AB05,AB07,AC03,BB05,BF03,BF15,5F040DA02,DB03,EC07,
    EC17,EC26,EJ01
    Expanded classification:  422
    Fixed keyword:  R097
    Citation:
    Title of invention:  CMOS output buffer
    Abstract:
```

        SUMMARY:Because an input signal is transmitted to gate electrode of
        CMOS output buffer by metal lines of low resistance by making CMOS
        output buffer have configuration, of an input waveform, a guard, incrementation
        of power consumption or drift of source voltage by breakthrough current
        or reference voltage can be prevented by incrementation of depending
        breakthrough current to get dull.
        (Machine Translation)

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    Priority country/date/number: (  ) [          ] (            )
```

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Classification of examiners decision/date: () [          ]
Final examinational transaction/date:       (withdrawal by no request for examination) [1988/10/25]
Examination intermediate record:
 (A63    1984/ 8/24,PATENT APPLICATION UTILITY MODEL REGISTRATION APPLICATION,07100:  )
 (A300   1988/10/13,MAKING OF FILE WRAPPER EXTRACTION LIST OF UNREQUEST FOR EXAMINATION,       :  )

*** Trial no/date            [          ] Kind of trial [] ***
 Demandant:      -
 Defendand:      -
 Opponent:       -
 Classification of trial decision of opposition/date: () [         ]
 Final disposition of trial or appeal/date:       () [         ]
 Trial and opposition intermediate record:

Registration intermediate record:

 Amount of annuities payment:     year
 Lapse date of right:   [         ]
 Proprietor:     -
```